WHAT IS CLAIMED IS:

1. A packet processing device for processing packets, comprising:

a plurality of packet processors each including packet input means to which a packet is input, internal information handover means for handing over internal information of the corresponding packet processor, packet computing means for computing the input packet in accordance with the internal information, and packet output means for outputting the computed packet; and

a communication line connecting said packet processors in series.

2. The packet processing device according to claim 1, wherein said internal information handover means hands over a value of a status flag as the internal information.

3. The packet processing device according to claim 1, wherein said internal information handover means hands over, as the internal information, address information of a program bank storing a packet processing program.

4. The packet processing device according to claim 1, wherein said internal information handover means

hands over, as the internal information, a computation result stored in a local register.

5. The packet processing device according to claim 1, wherein said internal information handover means sets handover timing for the internal information.

6. The packet processing device according to claim 1, wherein said internal information handover means selectively hands over the internal information.

7. A packet processor for processing packets, comprising:

packet input means to which a packet is input;

internal information handover means for handing over internal information of the packet processor;

packet computing means for computing the input packet in accordance with the internal information; and

packet output means for outputting the computed packet.